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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,775	09/29/2003	Keiji Mabuchi	09792909-5695	2481

26263 7590 10/15/2008

SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER	
HOGUE, DENNIS A	
ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
10/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,775	MABUCHI, KEIJI	
	Examiner	Art Unit	
	DENNIS HOGUE	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11,13-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11,13-18 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the second Office Action based on the 10/673,775 application filed 9/29/2003. Claims 6-11, 13-18, and 20-26 as amended are currently pending and have been considered below. Claims 1-5, 12, and 19 have been cancelled.

Drawings

2. The replacement drawings of Figures 11 and 12 were received on 7/11/2008. These drawings are accepted, and the objection to the drawings is withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 6-11, 13-18, and 20-26 have been considered but are moot in view of the new ground(s) of rejection.

4. Regarding applicant's argument on page 11 of the amendment received on 7/11/2008, which is directed at the combination of Rhodes (CMOS) with Mori et al. (CCD), the argument is not persuasive. The applicant argues that teaching relevant to a CMOS image sensor cannot be combined with teaching relevant to a CCD image sensor for the reason that CMOS and CCD technology are different technologies with different concerns and problems. This is in general not true. It is true that CMOS and CCD image sensors are different technologies, and each has certain aspects that are unique to each technology. However, both technologies are integrated circuit image sensor technologies and as such have many aspects in common. For example, the photodiode and transfer gate in both technologies are similar and teaching related to the

photodiode or transfer gate is relevant to both technologies. The main difference between the two technologies is that CCD image sensors comprise CCD shift registers that shift packets of charge to a common sense amplifier whereas CMOS image sensors have the sense amplifier incorporated into each pixel. That is, it is not fair to state that teaching applied to a CMOS image sensor may not apply to a CCD image sensor simply because the sensors are of a different type. The examiner mentions this because of the teachings of Morimoto (US Patent 5,729,287) and Shinji (Japanese Patent Application Publication JP-2000-022126), both of which teach that applying a reduced voltage to the substrate during read out of the pixel reduces the readout voltage required and thus the power consumption of the device. In the examiner's opinion, this teaching applies equally well to CCD or CMOS image sensors. Neither of these references is used in the current rejections, but they are relevant to what the examiner thinks the applicant is intending to claim in claim 6.

Remarks

5. Regarding claim 6, based on the language "(d) voltage control unit for applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout section", the examiner believes that applicant perhaps intends to claim that the voltage control unit applies a first predetermined substrate bias voltage to said well region prior to reading out of the signal charge by said readout section, and upon reading out of the signal charge by said readout section, applies a second predetermined substrate bias voltage to said well region, wherein the second

predetermined substrate bias voltage is different from the first predetermined substrate bias voltage. If this is the applicant's intent, then the applicant should change the language to better reflect that intent. As the language is currently drawn, an image sensor that applies a predetermined substrate bias voltage at all times reads on the claim.

6. Also regarding claim 6, if applicant's intent is as stated above, then the applicant should consider the Morimoto (US Patent 5,729,287) and Shinji (Japanese Patent Application Publication JP-2000-022126) references, both of which teach that applying a reduced voltage to the substrate during read out of the pixel reduces the readout voltage required and thus the power consumption of the device. In the examiner's opinion, this teaching applies equally well to CCD or CMOS image sensors.

7. Regarding claim 20, the examiner wonders if the clause (iv) is correct because it does not match the last clause under the method part of the claim. The examiner mentions this because it appears that claim 20 may be intended to be the method counterpart to claim 6, in the same way that claim 25 is the method counterpart to claim 13.

8. Regarding claims 20 and 25, both of these claims are rejected under USC 112 for combining an apparatus and a method in a single claim. The examiner recommends incorporating (a) and (b) hardware limitations into the preamble, getting rid of the first "comprising", and converting items (i) through (iv) to method steps after the second "comprising".

9. Regarding the language "substrate bias voltage" in claims 1, 8-10, 13, 15-17, 20, and 22-25, "substrate bias voltage" is interpreted to include a bias voltage applied to the substrate or a bias voltage applied to the well. The reason for this is because claim 9 states that each pixel row is formed in a single well, and an independent substrate bias voltage is applied to each row. If the wells for each row are built on a single substrate, such as shown in Fig. 4, then a substrate voltage that is directly applied to the substrate of a row cannot be independent of the substrate voltage applied to the substrate of a different row because the rows are built on the same substrate. Rather, the examiner concludes that the substrate voltage is applied directly to the well of a row so that it may be independent of the bias voltage applied to other rows.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 20-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The reason for this is that the claims combine an apparatus and a method. See MPEP 2173.05(p):

> II. PRODUCT AND PROCESS IN THE SAME CLAIM
>
> A single claim which claims both an apparatus and the method steps of using the apparatus is indefinite under 35 U.S.C. 112, second paragraph. *> IPXL Holdings v. Amazon.com, Inc., 430

F.2d 1377, 1384, 77 USPQ2d 1140, 1145 (Fed. Cir. 2005);< Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990) *>(< claim directed to an automatic transmission workstand and the method * of using it * held ** ambiguous and properly rejected under 35 U.S.C. 112, second paragraph>)<. Such claims *>may< also be rejected under 35 U.S.C. 101 based on the theory that the claim is directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. Id. at 1551.

Regarding claims 20 and 26, the examiner recommends incorporating (a) and (b) hardware limitations into the preamble, getting rid of the first "comprising", and converting items (i) through (iv) to method steps after the second "comprising".

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 6 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Chi et al. (US Patent 5,587,596).

Regarding claim 6, Chi et al. teach a solid-state complementary metal-oxide semiconductor type image pickup device (active pixel sensor cell 100, col. 1 lines 35-41, col. 2 lines 56-66, Figs. 1 and 2), comprising: a semiconductor substrate (semiconductor substrate 100) having a well region formed thereon (p-well 112); and a

pixel unit (see Fig. 3) comprising a plurality of pixels (cell 100) on the semiconductor substrate (see Fig. 3 which shows several pixels on a common substrate), each pixel in the pixel unit including (a) a photoelectric conversion element formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (p-well 112 and n-substrate 110 form a photodiode, Fig. 2; during image integration, photons strike the surface of p-well 112 and as a result create a number of electron-hole pairs, col. 3 lines 29-31; the photogenerated electrons are in turn attracted to the junction between the p-well 112 and n-substrate 110 where many of these carriers diffuse over to the substrate 110 and in turn raise the potential of p-well 112, col. 3 lines 34-38); (b) a readout section (pixels transistor 114) formed in said well region (see Fig. 2) for reading out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (as the potential of p-well 112 rises, the threshold voltage of pixel transistor 114 falls due to the body effect, col. 3 lines 39-41; as a result, when the pixel transistor 114 is read, the magnitude of the current output by drain region 118 will be approximately proportional to the change in the potential of the p-well 112 which in turn is proportional to the number of photons striking the surface of p-well 112, col. 3 lines 41-45; the signal from the pixel is output when a voltage Vrow is applied to the conductive gate 124, col. 3 lines 47-52); (c) a node connecting the photo electric conversion element through the readout section (the p-well 112 is a node that connects the photodiode and the readout section); and (d) voltage control unit (Vcc power supply circuitry) for applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout

section (the substrate is connected to Vcc, see Fig. 2; the substrate is connected to the predetermined substrate bias voltage of Vcc upon reading out of the signal charge by said readout section because the substrate 110 is always connected to Vcc; the voltage applied to the substrate 110 is also applied to the p-well 112 because the p-well 112 and the substrate 110 are in contact, see Fig. 2).

Regarding claim 11, Chi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said solid-state image pickup device each pixel also includes a pixel transistor for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (as the potential of p-well 112 rises, the threshold voltage of pixel transistor 114 falls due to the body effect, col. 3 lines 39-41; as a result, when the pixel transistor 114 is read, the magnitude of the current output by drain region 118 will be approximately proportional to the change in the potential of the p-well 112 which in turn is proportional to the number of photons striking the surface of p-well 112, col. 3 lines 41-45; the signal from the pixel is output when a voltage Vrow is applied to the conductive gate 124, col. 3 lines 47-52).

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 6, 7, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Koizumi et al. (US Patent 6,661,459).

Regarding claim 6, Koizumi et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (CMOS image sensor, see Fig. 12), comprising: a semiconductor substrate (n-type substrate 101, Fig. 3) having a well region formed thereon (p-well 102); and a pixel unit (3x3 pixel area of the CMOS image sensor, see Fig. 12) comprising a plurality of pixels (the CMOS image sensor of Fig. 12 comprises a 3 by 3 matrix of pixels, each pixel having the structure of Fig. 3) on the semiconductor substrate (the pixels are formed on n-type semiconductor substrate 101), each pixel in the pixel unit including (a) a photoelectric conversion element (N semiconductor region 104 and P semiconductor region 105 form a photodiode) formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (in response to the incident light, the electrons generated by photoelectric conversion are accumulated in the n-layer of the photodiode, col. 5 lines 43-45); (b) a readout section (transfer MOS transistor, col. 5 lines 24-29) formed in said well region for reading out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (n-layer 107 and n-type bypass region 106 are formed in p-well 102, see Fig. 3; together with the gate electrode 103 these components form the transfer MOS transistor; after the lapse of a predetermined

accumulation time, a positive voltage is applied to the control electrode of the transfer MOS transistor, thereby transferring the accumulated charge in the n-layer 104 to the diffusion region 107, col. 5 lines 46-51); (c) a node connecting the photo electric conversion element through the readout section (this is interpreted as "a node connecting the photo electric conversion element **to** the readout section" because the applicant's disclosed readout section is a FET; n-layer 104 connects the photodiode to the transfer MOS transistor, see Fig. 3), and (d) voltage control means for applying a substrate bias voltage to said well region upon reading out of the signal charge by said readout section (a substrate bias voltage is applied to the substrate, col. 2 line 23; the substrate is connected to the predetermined substrate bias voltage of Vs upon reading out of the signal charge by said readout section because the substrate 101 is always connected to Vs; that is, Koizumi does not teach changing of the substrate voltage at any time; the voltage applied to the substrate 101 is also applied to the p-well 102 because the p-well 102 and the substrate 101 are in contact, see Fig. 3).

Regarding claim 7, Koizumi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said plurality of pixels are arranged in a two-dimensional array on said semiconductor substrate (see Fig. 12, which displays a 3 by 3 matrix of pixels).

Regarding claim 11, Koizumi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said solid-state image pickup device each pixel (see Fig. 3) also includes a pixel transistor (transistor 110) for converting the signal charge read out from said photoelectric

conversion element into an electric signal and outputting the electric signal to a signal line (amplifying MOS transistor 110 receives the signal from the floating diffusion region 107 and amplifies the signal, outputting the signal to a vertical transfer line through the select transistor 111, see Fig. 3).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) in view of Rhodes (US Patent 6,825,878).

Regarding claim 8, Koizumi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 7. However, Koizumi et al. do not teach that said well region is electrically integral in a region of said semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array with the image sensor of Koizumi et al. so that the complexity of the device would be reduced. This would reduce the cost of the device. That is, one of ordinary skill would recognize that it is simpler to construct a single well for all of the pixels, rather than individual wells for each pixel or a subset of pixels.

18. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) as applied to claim 7 above, and further in view of Chi (US Patent 6,501,109).

Regarding claim 9, Koizumi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 7. However, Koizumi et al. do not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Koizumi et al. so that the well for each row to be individually pulsed for enhancement of the pixel dynamic range. This would increase the flexibility of the camera. It would be very useful for

incorporating a rolling shutter application wherein some rows are exposed while other rows are being read out. Such an application increases the readout speed of the sensor.

19. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) as applied to claim 6 above, and further in view of Merrill (US Patent 5,747,840).

Regarding claim 10, Koizumi et al. teach the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said well region is a p-type well region (the well is p-well 102). However, Koizumi et al. do not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one layer and a negative voltage to the other layer (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Koizumi et al. so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

20. Claims 13, 14, 18, 20, 21, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) in view of Murakami et al. (US Patent 6,486,460).

Regarding claims 13 and 25, Koizumi et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (CMOS image sensor, see Fig. 12), comprising: a semiconductor substrate (n-type substrate 101, Fig. 3) having a well region formed thereon (p-well 102); and a pixel unit (3x3 pixel area of the CMOS image sensor, see Fig. 12) comprising a plurality of pixels (the CMOS image sensor of Fig. 12 comprises a 3 by 3 matrix of pixels, each pixel having the structure of Fig. 3) on the semiconductor substrate (the pixels are formed on n-type semiconductor substrate 101), each pixel in the pixel unit including (a) a photoelectric conversion element (N semiconductor region 104 and P semiconductor region 105 form a photodiode) formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (in response to the incident light, the electrons generated by photoelectric conversion are accumulated in the n-layer of the photodiode, col. 5

lines 43-45); (b) a readout section (transfer MOS transistor, col. 5 lines 24-29) formed in said well region for reading out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (n-layer 107 and n-type bypass region 106 are formed in p-well 102, see Fig. 3; together with the gate electrode 103 these components form the transfer MOS transistor; after the lapse of a predetermined accumulation time, a positive voltage is applied to the control electrode of the transfer MOS transistor, thereby transferring the accumulated charge in the n-layer 104 to the diffusion region 107, col. 5 lines 46-51); (c) a node connecting the photo electric conversion element through the readout section (this is interpreted as "a node connecting the photo electric conversion element **to** the readout section" because the applicant's disclosed readout section is a FET; n-layer 104 connects the photodiode to the transfer MOS transistor, see Fig. 3), and (d) voltage control unit for applying a substrate bias voltage to said well region (a substrate bias voltage is applied to the substrate, col. 2 line 23). However, Koizumi et al. do not teach a voltage control means that changes the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element.

Murakami et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (image sensing device 1 comprises multiple sensor elements 2 that are CMOS sensing means, col. 5 lines 23-25, 36-39), comprising: a semiconductor substrate (the sensing means 2 are built on a semiconductor substrate, col. 5 lines 43-48; see Fig. 19A P- semiconductor region 221) having a well region formed thereon (P semiconductor region 222); and a pixel unit (solid-state image

sensing device 1) comprising a plurality of pixels (sensing means 2) on the semiconductor substrate (the pixels are formed on a P- type semiconductor substrate 221, Fig. 2), each pixel in the pixel unit including (a) a photoelectric conversion element (N semiconductor region 224 and P semiconductor region 222 form a photodiode) formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (photoelectric conversion section 201 accumulates a signal charge proportional to the amount of incident light, col. 13 lines 61-64); and (d) voltage control means (control means 5) for applying a substrate bias voltage to said well region (the substrate voltage is applied to the substrate 221; it is also applied to the p-well 222 because the p-well 222 is in contact with the substrate 221, see Fig. 19A) and changing the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the control means 5 is composed so that it controls the substrate voltage of the sensing means 2 to vary when varying the amount of accumulable charge, col. 5 lines 43-49; in other words, the substrate voltage is changed during the exposure portion of the imaging cycle so that the saturation voltage of the photodiode changes and the dynamic range is expanded; Figs 9 and 11 show cases where the substrate voltage is changed once during exposure; Figs. 13 and 15 show cases where the substrate voltage is changed three times during exposure; Fig. 17 shows a case where the substrate voltage is continuously changed during exposure). By changing the substrate voltage during exposure, the capacity of the photodiode is changed, which changes the saturation level of the photodiode, and

thereby achieves an improvement in dynamic range. Dynamic range is the range of the light intensity levels for a given exposure that a pixel can accurately capture.

Therefore, it would be obvious to one of ordinary skill in the art to combine the substrate voltage changing means of Murakami et al. with the CMOS image sensor of Koizumi et al. so that the dynamic range of the image sensor could be improved. This would allow a user to capture a wider range of light intensity levels in his or her photographs, thus improving the quality of the images.

Regarding claim 20, Koizumi et al. teach a method for driving a solid-state image pickup device (CMOS image sensor, see Fig. 12) comprising (a) a semiconductor substrate (n-type substrate 101, Fig. 3) having a well region formed thereon (p-well 102); and (b) a pixel unit (3x3 pixel area of the CMOS image sensor, see Fig. 12) comprising a plurality of pixels (the CMOS image sensor of Fig. 12 comprises a 3 by 3 matrix of pixels, each pixel having the structure of Fig. 3) on the semiconductor substrate (the pixels are formed on n-type semiconductor substrate 101), each pixel in the pixel unit including (i) a photoelectric conversion element (N semiconductor region 104 and P semiconductor region 105 form a photodiode) formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (in response to the incident light, the electrons generated by photoelectric conversion are accumulated in the n-layer of the photodiode, col. 5 lines 43-45); (ii) a readout section (transfer MOS transistor, col. 5 lines 24-29) formed in said well region for reading out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (n-layer 107 and n-type bypass region 106 are formed

in p-well 102, see Fig. 3; together with the gate electrode 103 these components form the transfer MOS transistor; after the lapse of a predetermined accumulation time, a positive voltage is applied to the control electrode of the transfer MOS transistor, thereby transferring the accumulated charge in the n-layer 104 to the diffusion region 107); (iii) a node connecting the photo electric conversion element through the readout section (this is interpreted as "a node connecting the photo electric conversion element **to** the readout section" because the applicant's disclosed readout section is a FET; n-layer 104 connects the photodiode to the transfer MOS transistor, see Fig. 3), and (iv) voltage control means for applying a substrate bias voltage to said well region (a substrate bias voltage is applied to the substrate, col. 2 line 23), said method comprising the steps of: converting light to a signal charge (in response to the incident light, the electrons generated by photoelectric conversion are accumulated in the n-layer of the photodiode, col. 5 lines 43-45); storing said signal charge during a charge storage period (in response to the incident light, the electrons generated by photoelectric conversion are accumulated in the n-layer of the photodiode, col. 5 lines 43-45); and applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout section during said readout period (a substrate bias voltage is applied to the substrate, col. 2 line 23; Koizumi teaches applying a fixed voltage to the substrate; therefore, Koizumi teaches applying a predetermined substrate voltage upon reading out of the signal charge during the readout period because Koizumi teaches applying a fixed substrate voltage at all times). However, Koizumi et al. do not teach a voltage control means that changes the

substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element.

Murakami et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (image sensing device 1 comprises multiple sensor elements 2 that are CMOS sensing means, col. 5 lines 23-25, 36-39), comprising: a semiconductor substrate (the sensing means 2 are built on a semiconductor substrate, col. 5 lines 43-48; see Fig. 19A P- semiconductor region 221) having a well region formed thereon (P semiconductor region 222); and a pixel unit (solid-state image sensing device 1) comprising a plurality of pixels (sensing means 2) on the semiconductor substrate (the pixels are formed on a P- type semiconductor substrate 221, Fig. 2), each pixel in the pixel unit including (a) a photoelectric conversion element (N semiconductor region 224 and P semiconductor region 222 form a photodiode) formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light (photoelectric conversion section 201 accumulates a signal charge proportional to the amount of incident light, col. 13 lines 61-64); and (d) voltage control means (control means 5) for applying a substrate bias voltage to said well region (the substrate voltage is applied to the substrate 221; it is also applied to the p-well 222 because the p-well 222 is in contact with the substrate 221, see Fig. 19A) and changing the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the control means 5 is composed so that it controls the substrate voltage of the sensing means 2 to vary when varying the amount of accumulable charge, col. 5 lines 43-49; in other words, the substrate voltage is

changed during the exposure portion of the imaging cycle so that the saturation voltage of the photodiode changes and the dynamic range is expanded; Figs 9 and 11 show cases where the substrate voltage is changed once during exposure; Figs. 13 and 15 show cases where the substrate voltage is changed three times during exposure; Fig. 17 shows a case where the substrate voltage is continuously changed during exposure). By changing the substrate voltage during exposure, the capacity of the photodiode is changed, which changes the saturation level of the photodiode, and thereby achieves an improvement in dynamic range. Dynamic range is the range of the light intensity levels for a given exposure that a pixel can accurately capture.

Therefore, it would be obvious to one of ordinary skill in the art to combine the substrate voltage changing means of Murakami et al. with the CMOS image sensor of Koizumi et al. so that the dynamic range of the image sensor could be improved. This would allow a user to capture a wider range of light intensity levels in his or her photographs, thus improving the quality of the images.

Regarding claims 14, 21, and 26, Koizumi et al. in view of Murakami et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 13, 20, and 25, wherein said plurality of pixels are in a two-dimensional array on said semiconductor substrate (see Koizumi Fig. 12; the CMOS image sensor is a 3x3 array of pixels).

Regarding claim 18, Koizumi et al. in view of Murakami et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 13, wherein each of said .plurality of pixels also includes a pixel

transistor (Koizumi: amplifying transistor 110) for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (amplifying transistor 110 converts the charge from the photodiode into a voltage and outputs the voltage signal through selection transistor 111 to a vertical transfer line, see Fig. 3).

21. Claims 15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) in view of Murakami et al. (US Patent 6,486,460) as applied to claims 14 and 21 above, and further in view of Rhodes (US Patent 6,825,878).

Regarding claims 15 and 22, Koizumi et al. in view of Murakami et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 14 and 21. However, Koizumi et al. in view of Murakami et al. does not teach that said well region is electrically integral in a region of said semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions.

Rhodes teaches that all of the pixels of the pixel portion of the image sensor are formed in a single well (col. 7 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array with the image sensor of Koizumi et al. in view of Murakami et al. so that the complexity of the device would be reduced. This would reduce the cost of the device. That is, one of ordinary skill would recognize that it is

simpler to construct a single well for all of the pixels, rather than individual wells for each pixel or a subset of pixels.

22. Claims 16 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) in view of Murakami et al. (US Patent 6,486,460) as applied to claims 14 and 21 above, and further in view of Chi (US Patent 6,501,109).

Regarding claims 16 and 23, Koizumi et al. in view of Murakami et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 14 and 21. However, Koizumi et al. in view of Murakami et al. does not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two- dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Chi et al. in view of Rhodes so that the well for each row to be individually pulsed for enhancement of the pixel dynamic range. This would increase the flexibility of the camera. It would be very useful for incorporating a rolling shutter application wherein some rows are exposed

while other rows are being read out. Such an application increases the readout speed of the sensor.

23. Claims 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent 6,661,459) in view of Murakami et al. (US Patent 6,486,460) as applied to claims 13 and 20 above, and further in view of Merrill (US Patent 5,747,840).

Regarding claims 17 and 24, Koizumi et al. in view of Murakami et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 13 and 20, wherein said well region is a p-type well region (p-well 102). However, et al. in view of Murakami et al. does not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one and a negative voltage to the other (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Koizumi et al. in view of Murakami et al. so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakagawa (Japanese Patent Application Publication JP-2000-022126) teaches an image sensor wherein applying a reduced voltage to the substrate during read out of the pixel reduces the readout voltage required and thus the power consumption of the device.

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS HOGUE whose telephone number is (571) 270-5089. The examiner can normally be reached on Mon. - Thurs., 8:00 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DH

Examiner

10/2/2008

/Lin Ye/

Supervisory Patent Examiner, Art Unit 2622